CLAIMS

What is claimed is:

1. A method of measuring an uncertainty window within which a target clock signal of an electronic device makes state transitions, the method comprising:

defining a time window between features of a first and second reference clock signals; and

comparing within the electronic device a plurality of cycles of the target clock signal to the reference clock signals to determine whether the target clock signal makes state transitions within the time window.

2. The method of measuring the uncertainty window as defined in claim 1 further comprising:

generating the first and second reference clock signals within the electronic device;

phase delaying the second reference clock signal more than the first reference clock signal; and

defining the time window between features of the first and second reference clock signals.

3. The method of measuring the uncertainty window as defined in claim 2 wherein defining the time window further comprises defining the time window between corresponding rising edges of the first and second reference clock signals.

4. The method of measuring the uncertainty window as defined in claim 1 wherein comparing the reference clock signals to the target clock signal further comprises:

phase detecting the first reference clock signal against the target clock signal to determine whether the target clock signal makes its state transition before or after the first reference clock signal;

phase detecting the second reference clock signal against the target clock signal to determine whether the target clock signal makes its state transition before or after the second reference clock signal, and wherein the target clock signal makes state transitions within the time window if those transitions are detected to be after the first reference clock signal and before the second reference clock signal.

5. A microprocessor, comprising:

a clock domain region having a target clock;

a jitter measurement circuit associated with the clock domain region; and

wherein the jitter measurement circuit measures an uncertainty window within which the cache clock makes state transitions.

6. The microprocessor as defined in claim 5 wherein the jitter measurement circuit further comprises:

a plurality of delay units creating a plurality of reference clock signals, each reference clock signal having the same frequency but differing in phase relationship; and

a measurement unit coupled to the plurality of reference clock signals and the target clock, and wherein the measurement unit compares the target clock to the plurality of reference clock signals to determine the uncertainty window of the target clock.

7. The microprocessor as defined in claim 6 wherein each of the delay unit further comprises an inverter chain having a programmable delay.

8. The microprocessor as defined in claim 7 wherein the inverter chain further comprises:

a coarse delay circuit coupled to the host clock, wherein the coarse delay circuit provides a programmable delay in a first time range; and

a fine delay circuit coupled to the coarse delay circuit, wherein the fine delay circuit provides a programmable delay in a second time range which is smaller than the first time range.

9. The microprocessor as defined in claim 8 wherein the coarse delay circuit further comprises:

a plurality of delay elements each having a delay input signal and a delay output signal, the plurality of delay elements coupled in series, and the first delay element having its delay input signal coupled to a host clock;

a multiplexer having a plurality of data inputs coupled one each to the delay output signals of the plurality of delay elements coupled in series; and

wherein the coarse delay circuit implements its programmable delay by coupling only one of the data inputs of the multiplexer to a data output of the multiplexer responsive a plurality of control signals applied to the multiplexer.

10. The microprocessor as defined in claim 9 wherein the delay elements of the coarse delay circuit further comprises four inverters coupled in series.

11. The microprocessor as defined in claim 9 wherein the plurality of delay elements of the coarse delay circuit further comprises sixteen delay elements.

12. The microprocessor as defined in claim 9 wherein the multiplexer having a plurality of data inputs further comprises a multiplexer having sixteen data inputs.

13. The microprocessor as defined in claim 9 wherein the coarse delay circuit implements a delay varying between 80 and 3100 picoseconds.

14. The microprocessor as defined in claim 8 wherein the fine delay circuit further comprises a of plurality of adjustable delay elements each having a delay input signal and a delay output signal, the plurality of adjustable delay elements coupled in series, and the first delay element having its delay input signal coupled to the coarse delay circuit.

15. The microprocessor as defined in claim 14 wherein the adjustable delay elements further comprise an inverter having a plurality of transistors that may be selectively added to increase the inverter's propagation speed.

16. The microprocessor as defined in claim 15 wherein the fine delay circuit implements delay ranging from 200 to 500 picoseconds.

17. The jitter measurement unit as defined in claim 6 further comprising a calibration unit configured to provide signals for calibration of the jitter measurement unit.

18. The microprocessor as defined in claim 17 wherein the calibration unit further comprises:

a plurality of inverter pairs coupled in series, and a first inverter pair in the series coupled to a clock signal, wherein a number of inverter pairs a propagating signals passes through in one period of the clock signal is indicative of speed of the inverter pairs in the calibration unit;

a second plurality of inverter pairs coupled to the clock signal;

a first tap signal coupled to the second plurality of inverters between a first inverter pair and a second inverter pair;

a second tap signal coupled to the second plurality of inverters after the second inverter pair; and

wherein the phase difference between the first and second tap signals is proportional to a known portion of the clock period.

19. A method of measuring an uncertainty window within which a target clock signal on a microprocessor die makes state transitions, the method comprising:

generating on the microprocessor die a first and second reference clock signals having the same frequency but differing in phase relationship;

defining a time window between features of the first and second reference clock signals;

comparing on the microprocessor die a plurality of cycles of the target clock signal to the reference clock signals to determine whether the target clock signal makes state transitions within the time window;

adjusting the time window; and

repeating the comparing step and adjusting step to determine the uncertainty window.

20. The method of measuring an uncertainty window as defined in claim 19 wherein generating the first and second reference clock signal on the microprocessor die further comprises:

coupling a core clock signal to a first adjustable delay chain;

delaying the core clock by a first length of time with the first adjustable delay chain to create the first reference clock signal;

coupling the core clock signal to a second adjustable delay chain; and

delaying the core clock by a length of time greater than the first length of time with the second adjustable delay chain to create the second reference clock signal.

21. The method of measuring an uncertainty window as defined in claim 20 wherein delaying the core clock with the first and second adjustable delay chain further comprises:

applying the core clock to a plurality of buffers coupled in series; and

adjusting a desired delay for each buffer of the plurality of buffers by controlling the amount of operational transistor area of buffer.

22. The method of measuring an uncertainty window as defined in claim 21 wherein applying the core clock to a plurality of buffers further comprises applying the core clock to a plurality of programmable delay inverting buffers.

23. The method of measuring an uncertainty window as defined in claim 19 wherein defining the time window further comprises defining the time window between corresponding low voltage to high voltage state transitions of the first and second reference clock signals.

24. The method of measuring an uncertainty window as defined in claim 19 wherein adjusting the time window further comprises adjusting the phase relationship of the first and second reference clock signals.

25. The method of measuring the uncertainty window as defined in claim 24 wherein adjusting the time window further comprises:

setting the time window smaller than an anticipated uncertainty window;

comparing the plurality of cycles of the target clock signal to the first and second reference clock signals; and

expanding the time window until in the comparison of the plurality of target clock cycles has substantially all the state transitions of the target clock signal within the time window.

26. The method of measuring an uncertainty window as defined in claim 24 wherein adjusting the time window further comprises:

setting the time window larger than an anticipated uncertainty window;

comparing the plurality of cycles of the target clock signal to the first and second reference clock signals;

contracting the time window until in the comparison of the plurality of target clock cycles has transitions of state outside the time window; then

expanding the time window until the comparison of the plurality of clock cycles has substantially all the state transitions occur within the time window.

27. A system for measuring an uncertainty window of a target clock signal of a microprocessor, the system comprising:

a measurement circuit on the die of the microprocessor;

an external measurement system coupled the measurement circuit by way of a scan chain of the microprocessor, and wherein the external measurement system executes software adapted to control the measurement circuit through the scan chain;

wherein the external measurement system is further adapted to adjust a phase relationship of a plurality reference clock signals having varying phase, the plurality of reference clock signals define a plurality of time windows between corresponding features; and

wherein the measurement circuit compares the target clock signal to the plurality of time windows to determine the uncertainty window of the target clock signal.

28. The system for measuring the uncertainty window as defined in claim 27 wherein the measurement circuit further comprises:

a plurality of delay units each coupled to a host clock and creating the plurality of reference clock signals by selectively phase delaying the host clock signal by each of the delay units; and

a measurement unit coupled to the plurality of reference clock signals and the target clock signal, and wherein the measurement unit compares the plurality of reference clock signals to the target clock signal to determine the uncertainty window.

29. The system for measuring the uncertainty window as defined in claim 28 wherein each of the plurality of delay units further comprises:

a coarse delay circuit coupled to the host clock, wherein the coarse delay circuit provides a programmable delay in a first time range; and

a fine delay circuit coupled to the coarse delay circuit, wherein the fine delay circuit provides a programmable delay in a second time range which is smaller than the first time range.

30. The system for measuring the uncertainty window as defined in claim 29 wherein the coarse delay circuit further comprises:

a plurality of inverter quadruplets comprising four inverters coupled in series, each inverter quadruplet having a delay input signal and a delay output signal, the plurality of inverter quadruplets coupled in series, and a first inverter quadruplet having its delay input signal coupled to the host clock;

a multiplexer having a plurality of data inputs coupled one each to the delay output signals of the plurality of inverter quadruplets; and

wherein the coarse delay circuit implements its programmable delay by coupling only one of the data inputs of the multiplexer to a data output of the multiplexer responsive a plurality of control signals applied to the multiplexer.

31. The system for measuring the uncertainty window as defined in claim 28 wherein the measurement unit further comprises a minimum/maximum unit coupled to the external system by way of the scan chain, and wherein the minimum/maximum unit is adapted to determine a minimum and maximum thermometer codes in each measurement run.

32. The system for measuring the uncertainty window as defined in claim 27 wherein the external measurement system further comprises a microcontroller adapted to execute software algorithms coupled to the measurement circuit by way of the scan chain.

33. In system for measuring on the die of the electronic device an uncertainty window within which a target clock signal may make a state transition, a method of calibrating a measurement circuit comprising:

generating a first and second calibration signal, each calibration signal having the same frequency, but differing in phase relationship by a known period of time;

phase locking an output signal of a programmable delay chain to the first calibration signal;

noting a number of programmable taps required to phase lock to the first calibration signal;

phase locking the output signal of the programmable delay chain to the second calibration signal;

noting the number of programmable taps required to phase lock to the second calibration signal;

attributing the difference in the number of taps to lock to the first and second calibration signal to the known period of time; and thereby

attributing to each tap a portion of the known period of time.

34. The method of calibrating a measurement circuit as defined in claim 33 wherein generating the first and second calibration signal further comprises:

applying a host clock signal to a first delay element having known propagation delay to create the first calibration signal; and

applying the first calibration signal to a second delay element having known propagation delay to create the second calibration signal.

35. The method of calibrating the measurement circuit as defined in claim 34 wherein applying the host clock to the first delay element and applying the first calibration signal to the second delay element further comprises:

applying the host clock and first calibration signal to respective inverter pairs having the same propagation delay.

36. The method of calibrating the measurement circuit as defined in claim 33 wherein the phase locking steps further comprise:

propagating a signal along the delay chain set up for a delay longer than required to lock to the respective signal;

comparing state transitions of the signal to the respective calibration signal; and if the comparison reveals the propagating signal makes a state transition after the respective calibration signal;

increasing the propagation speed along the delay chain; and

repeating the comparing step and the increasing the propagation speed step until the signal makes a state transition at substantially the same time as the respective calibration signal.

37. The method of calibrating the measurement circuit as defined in claim 33 wherein noting the number of programmable taps further comprises shifting tap information off the die of the electronic device by way of a serial communication pathway.

38. The method of calibrating the measurement circuit as defined in claim 37 wherein shifting the tap information off the die further comprises shifting the tap information off the die by way of a scan chain.

39. A microprocessor comprising:

a core region adapted to execute software routines;

a cache region acting as a working memory for the core region, and the cache region also having a cache clock; and

a measurement means on the microprocessor die for determining skew and jitter of the cache clock.

40. The microprocessor as defined in claim 39 wherein the measurement means further comprises:

a reference signal generating means for creating a reference clock signal; and

a comparison means for comparing the reference clock signal to the cache clock to determine the skew and jitter of the cache clock.

41. The microprocessor as defined in claim 40 wherein the reference signal generating means further comprises:

an adjustable delay means coupled to a host clock for providing an adjustable time delay of the host clock signal; and

a control means coupled to the adjustable delay means and to a scan chain, wherein the control means adjusts the time delay of the adjustable delay means responsive to commands communicated over the scan chain.

42. The microprocessor as defined in claim 41 wherein the adjustable delay means further comprises:

a coarse delay means coupled to the host clock for providing an adjustable time delay having a first range; and

a fine delay means coupled to the coarse delay means for providing an adjustable delay having a range smaller than that of the first range.

43. The microprocessor as defined in claim 40 wherein the comparison means further comprises:

a phase detection means coupled to the reference clock signal and the cache clock, and wherein the phase detection means for detecting the phase relationship between the reference clock signal and the cache clock; and

a means for determining the maximum and minimum detected phase relationship.

44. The microprocessor as defined in claim 40 wherein the measurement means further comprises a calibration means for generation a plurality of calibration signals, the calibration means coupled to the reference signal generating means.

45. A method for determining an uncertainty window within which a target clock signal of an electronic device makes state transitions, the method comprising:

generating on a microprocessor die a first, second, third and fourth reference clock signals having the same frequency but differing in phase relationship;

defining a first time bin between respective features of the first and second reference clock signals, defining a second time bin between respective features of the second and third reference clock signals, and defining a third time bin between respective features of the third and fourth reference clock signals;

comparing on the microprocessor die a plurality of cycles of the target clock signal to the reference clock signals to determine in which bin the target clock signal makes it state transitions;

adjusting the phase relationship of at least one of the reference clock signals, and thereby adjusting the time width of at least one time bin; and

repeating the adjusting step and the comparing step until the uncertainty window is determined.

46. The method of measuring an uncertainty window as defined in claim 45 wherein generating the first, second, third and fourth reference clock signals on the microprocessor die further comprises:

coupling a core clock signal to a first adjustable delay chain;

delaying the core clock by a first length of time with the first adjustable delay chain to create the first reference clock signal;

coupling the core clock signal to a second adjustable delay chain;

delaying the core clock signal by a second length of time greater than the first length of time with the second adjustable delay chain to create the second reference clock signal;

coupling the core clock signal to a third adjustable delay chain;

delaying the core clock signal by a third length of time greater than the second length of time with the third adjustable delay chain to create the third reference clock signal;

coupling the core clock signal to a fourth adjustable delay chain; and

delaying the core clock signal by a fourth length of time greater than the second length of time with the fourth adjustable delay chain to create the fourth reference clock signal.

47. The method of measuring an uncertainty window as defined in claim 46 wherein delaying the core clock with the first, second, third and fourth adjustable delay chain further comprises:

applying the core clock to a plurality of buffers coupled in series; and

adjusting a desired delay for each buffer of the plurality of buffers by controlling the amount of transistor area of buffer.

48. The method of measuring an uncertainty window as defined in claim 47 wherein applying the core clock to a plurality of buffers further comprises applying the core clock to a plurality of programmable delay inverting buffers.

49. The method of measuring an uncertainty window as defined in claim 45 wherein defining the time window further comprises defining the time window between corresponding low voltage to high voltage state transitions of the first and second reference clock signals, second and third reference clock signals, and the third and fourth reference clock signals.

50. The method of measuring an uncertainty window as defined in claim 45 wherein adjusting the time bins further comprises adjusting the phase relationship of at least one of the first, second, third and fourth reference clock signals.

51. The method of measuring the uncertainty window as defined in claim 50 wherein adjusting the time bins further comprises:

setting at least one time bin smaller than an anticipated uncertainty window;

comparing the plurality of cycles of the target clock signal to the at least one time bin; and

expanding the at least one time bin until in the comparison of the plurality of target clock cycles has substantially all the state transitions of the target clock signal within the at least one time bin.

52. The method of measuring an uncertainty window as defined in claim 50 wherein adjusting the time bin further comprises:

setting at least one time bin larger than an anticipated uncertainty window;

comparing the plurality of cycles of the target clock signal to the at least one time bin;

contracting the time width of the at least one time bin until in the comparison of the plurality of target clock cycles has transitions of state outside the at least one time bin; then

expanding the time window until the comparison of the plurality of clock cycles has substantially all the state transitions occur within the at least one time bin.

53. A microprocessor, comprising:

a cache region having a cache clock;

a jitter measurement circuit associated with the cache region, wherein the jitter measurement circuit measures an uncertainty window within which the cache clock makes state transitions;

wherein the jitter measurement circuit further comprises:

four delay units creating a four reference clock signals, each reference clock signal having the same frequency but differing in phase relationship;

a measurement unit coupled to the four reference clock signals and the cache clock, and wherein the measurement unit compares the cache clock to the plurality of reference clock signals to determine the uncertainty window of the cache clock; and

a calibration unit coupled to the delay unit and configured to provide signals for calibration of the jitter measurement unit.

54. The microprocessor as defined in claim 53 wherein each of the delay unit further comprises an inverter chain having a programmable delay.

55. The microprocessor as defined in claim 54 wherein the inverter chain further comprises:

a coarse delay circuit coupled to the host clock, wherein the coarse delay circuit provides a programmable delay in a first time range; and

a fine delay circuit coupled to the coarse delay circuit, wherein the fine delay circuit provides a programmable delay in a second time range which is smaller than the first time range.

56. The microprocessor as defined in claim 55 further comprising:

said coarse delay circuit provides a programmable delay in the range of 80 to 3100 picoseconds; and

said fine delay circuit provides a programmable delay in a range of 200 to 500 picoseconds.

57. The microprocessor as defined in claim 55 wherein the coarse delay circuit further comprises:

sixteen inverter quadruplets each having a delay input signal and a delay output signal, the sixteen inverter quadruplets coupled in series, and a first inverter quadruplet having its delay input signal coupled to a host clock;

a multiplexer having a sixteen data inputs coupled one each to the delay output signals of the inverter quadruplets; and

wherein the coarse delay circuit implements its programmable delay by coupling only one of the data inputs of the multiplexer to a data output of the multiplexer responsive a plurality of control signals applied to the multiplexer.

58. The microprocessor as defined in claim 55 wherein the fine delay circuit further comprises eight adjustable delay elements each having a delay input signal and a delay output signal, the plurality of adjustable delay elements coupled in series, and the first delay element having its delay input signal coupled to the coarse delay circuit.

59. The microprocessor as defined in claim 58 wherein the adjustable delay elements further comprise an inverter having a plurality of transistors that may be selectively added to increase the inverter's propagation speed.

60. The microprocessor as defined in claim 53 wherein the calibration unit further comprises:

thirty five inverter pairs coupled in series, and a first inverter pair in the series coupled to a clock signal, wherein a number of inverter pairs a propagating signals passes through in one period of the clock signal is indicative of speed of the inverter pairs in the calibration unit;

two inverter pairs coupled to the clock signal;

a first tap signal coupled to the inverters between a first inverter pair and a second inverter pair;

a second tap signal coupled to the two inverters after the second inverter pair; and

wherein the phase difference between the first and second tap signals is proportional to a known portion of the clock period.

61. The microprocessor as defined in claim 53 wherein the measurement unit further comprising:

a phase detection circuit coupled to the four reference clock signals and the cache clock which compares the four reference clock signals and generates a thermometer code for each such comparison; and

a min/max unit coupled to the phase detection unit and also to a scan chain, the min/max united adapted to record the minimum and maximum values produced by said phase detection circuit, and wherein the min/max unit further adapted to ship the minimum and maximum values off the microprocessor by way of the scan chain.